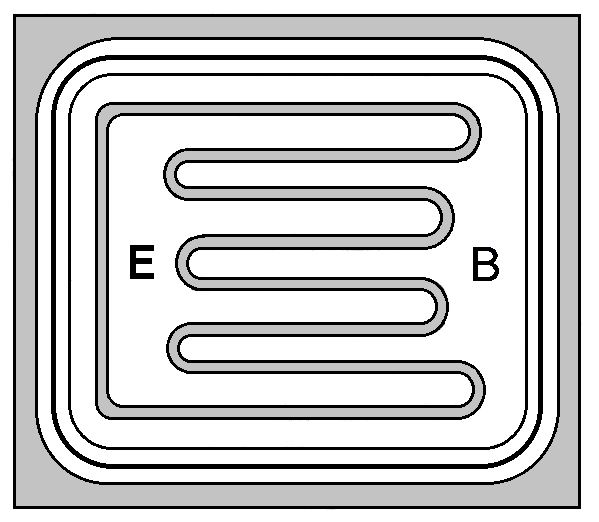
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.099”**

**.080”**



**Top Material: Si**

**Backside Material: CrNiAg**

**Bond Pad Size: .004” min.**

**Backside Potential: Collector**

**Mask Ref: CP611**

**APPROVED BY: DK DIE SIZE .080” X .099” DATE: 5/12/16**

**MFG: CENTRAL SEMI THICKNESS .012” P/N: TIP42C**

**DG 10.1.2**

#### Rev B, 7/19/02